REMARKS

This paper is in response to the Office Action mailed on January 29, 2004.

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 1-36 remain pending in this application.

Information Disclosure Statement

Applicant submitted a Supplemental Information Disclosure Statement and a 1449 Form on January 9, 2001. Applicant respectfully requests that and initialed copy of the 1449 Form be returned to Applicants' Representatives to indicate that the cited references have been considered by the Examiner.

Reservation of the Right to Swear Behind Documents

Applicant maintains its right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited documents are not to be interpreted as admissions that the documents are prior art.

§103 Rejection of the Claims

Claims 1-36 were rejected under 35 USC § 103(a) as being unpatentable over Madhaven et al. (U.S. Patent No. 5,675,545) in view of Ho, William (U.S. Patent No. 6,421,814) and Ho et al. (U.S. Patent No. 6,009,251). Applicant respectfully traverses and asserts that a *prima facie* case of obviousness has not been made.

The Office Action stated that as per claims 1 and 9, Madhavan discloses a cell design method and design system for designing and testing semiconductor memory with feature limitations substantially similar to the claimed invention (Abstract and "Summary of the Invention"). The Office Action alleges that according to Madhavan, the design apparatus includes global files for global variables and design data relating to layout or schematics layout and connectivity data of the functional block, a plurality of cell configuration files or claimed local files, each relating a plurality of local variables to the global variables in system files (Figs. 9, 1 0-1 1, col. 2, lines 27-44, col. 5, line 50 to col. 6, line 47, col. 8, lines 3 1 50, for example),

and a plurality of cells, each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells, including layout of the hierarchical semiconductor structure in accordance with parameters in the local files (Figs. 5-10, col. 6, line 48 to col. 8, line 50). The Examiner admits that Madhavan does not expressly disclose geometric variables related to physical layout in a hierarchical manner as claimed. The Examiner has agreed with Applicant that Madhavan and Ho ('814) fail to disclose or teach geometric variables related to the physical layout of a hierarchical semiconductor structure as recited in the claims (pages 10- 1 2).

However, the Office Action states that one in the art at the time the invention was made would have found Madhavan physical semiconductor memories in the integrated circuit area could have geometric shapes or sizes taking geometric parameter values, occupied in the chip placement area such that the hierarchical placement of cells is on the semiconductor substrate. The Office Action states that Ho ('814) teaches geometrical layout variables or parameters and such relations in geometrical layout data for physical design with faster and better layout in integrated circuit design (Background of the Invention, col. 1, lines 48-60, Fig. I B, col. 5, lines 3 3 -60). The Office Action states that Ho ('25 1) also teaches a net list for geometry and subcell design with local geometry and parent references for hierarchical cell layout design and cell interconnection verification (Figs. 2-4, col. 3, lines 25-67, col. 7, lines 7-36, col. 8, line 29 to col. 10, line 43, for example) in order to reduce verification time for cell layout as taught in Ho.

The Office Action then concludes that this would motivate practitioner in the art at the time of the invention was made to use Ho teaching of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Madhavan to improve layout processing time and faster in circuit design verification and testing as in Madhavan.

Ho ('251) appears to teach a layout verification process that operates on an integrated circuit design to reduce the layout verification process period required of a circuit designer. Ho ('251) teaches a layout verification method that includes design rule checking and layout versus schematic verification.

Ho ('251) appears to disclose a method and system for layout verification of an integrated circuit design using reusable subdesigns. Many custom designed integrated circuits, e.g.,

application specific integrated circuits (ASICs), are designed and fabricated using a number of computer implemented automatic design processes. Within these processes, a high level design language (e.g., HDL or VHDL) description of the integrated circuit can be translated by a computer system into a netlist of technology specific gates and interconnections there between. At this point the design is at the transistor level. The cells of the netlist are then placed spatially in an integrated circuit layout by a computer implemented placer and the connections between the cells are then routed through the appropriate places of the layout by a computer implemented router. Once the design has been placed and routed, circuit designers run a battery of tests on the result (e.g., geometry and connectivity data) to verify that the design meets specific design rules and matches logically with the schematic design. These tests are performed by a computer in a process called layout verification.

Ho ('251) appears to disclose a computer implemented method of verifying the layout of an integrated circuit design, the computer implemented method comprising the steps of: a) receiving a stream of layout information representing an integrated circuit layout design, the stream of information comprising a plurality of subcell designs having parent-child relationships; b) comparing names of the subcell designs against a history database and parsing and storing into a new database only those subcell designs that are not found within the history database, the history database representing previously parsed subcell designs; c) from the new and history databases, constructing a hierarchical tree of the subcell designs from the parent-child relationships; d) selecting a selected subcell design from the hierarchical tree; e) comparing the selected subcell design to indications within a validation store and performing design rule verification on the selected subcell design only if the selected subcell design is not indicated within a validation store, otherwise skipping the selected subcell design and obtaining a next selected subcell design; f) performing steps d)-e) for each subcell design of the hierarchical tree and generating a design rule verification report on the integrated circuit layout; and g) storing the geometry of each subcell design selected at step d) into the validation store that passed design rule verification. Combining this teaching with the other cited prior art would teach away from Applicant's claimed invention, since Ho ('251) would require both new and history databases.

A factor cutting against a finding of motivation to combine or modify the prior art is when the prior art teaches away from the claimed combination. A reference may be said to teach

away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path the applicant took. *In re Gurley*, 27 F.3d 551, 31 USPQ 2d 1130, 1131 (Fed. Cir. 1994); *United States v. Adams*, 383 U.S. 39, 52, 148 USPQ 479, 484 (1966); *In re Sponnoble*, 405 F.2d 578, 587, 160 USPQ 237, 244 (C.C.P.A. 1969); *In re Caldwell*, 319 F.2d 254, 256, 138 USPQ 243, 245 (C.C.P.A. 1963).

Independent claim 1 of the present application is directed to a system for populating parameters of design cells defining a physical layout of a hierarchical semiconductor structure comprising: a global file of global geometric variables relating to a physical layout of element blocks of the hierarchical semiconductor structure; a plurality of local files, each local file containing parameters relating a plurality of local variables to the global geometric variables; and, a plurality of programmable design cells, each cell corresponding to a local file and having a set of parameters created by relating the corresponding local variables within a local file to appropriate global geometric variables from the global file such that changes of global geometric variables in the global file may cause changes in the design cells for the physical layout of the hierarchical semiconductor structure in accordance with parameters in the local files.

Thus Applicant's invention is directed to a system for populating parameters of design cells defining a physical layout of a hierarchical semiconductor structure, whereas Ho ('251) is directed to a computer implemented method of verifying the layout of an integrated circuit design.

Further, the combination of Madhaven with Ho and Ho ('251) is not proper since there is no suggestion to combine the cited references as proposed in the Office Action, because there is no reasonable expectation for success of the proposed combination. The Office Action states that

"[t]his would motivate practitioner in the art at the time of the invention was made to use Ho teaching of geometrical layout file and geometrical shape variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Madhaven to better improve and faster layout processing in circuit design and testing as in Madhaven."

Applicant can not find a teaching or suggestion for using a geometrical layout file and geometrical shape variables in hierarchical relationships for a physical design of an integrated circuit disclosed in Madhaven as proposed in this quote. Madhaven deals with "an improved technique of assembling databases of complex circuit blocks that are being combined on a single integrated circuit chip to form a specific system architecture." Underlining added. See, column 83, lines 47- 49.

Further, Applicant can not find where Madhaven discloses a method and system that could use Ho and Ho ('251) geometric variables for the physical layout of a hierarchical semiconductor structure. Combining Ho and Ho ('251) device parameters with Madhaven's interconnection of circuit blocks approach would result in extraneous data for Madhaven's system and method, since Madhaven appears not to deal with an integrated circuit at the geometric and physical level of these geometric variables. Applicant can not find in the cited references or in the Office Action any reasons that would indicate that the Ho and Ho ('251) device parameters could be utilized in Madhaven's method and system, as proposed by the Office Action.

The Office Action stated "[p]ractitioner in the art at the time of the invention was made would have found Madhaven physical semiconductor memories in the integrated circuit area could have geometric shapes or sizes taking geometric parameter values, occupied in the chip area such that the chip could be tested. Such geometrical feature is also well-known in the semiconductor circuit design." The fact that semiconductor memories have geometrical features does not teach or suggest that Madhaven deals with the semiconductor memories at the physical layout of a semiconductor structure level or that Madhaven's method and apparatus can use geometric variables related to the physical layout of a semiconductor structure as recited in claim 1. The Office Action has provided no objective reference or a specific reason to support the proposition that Madhaven can use Ho and Ho ('251) geometric parameters. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. (Underlining added.) Since no reasonable expectation of success has been provided for the combination of Madhaven with Ho and Ho ('251) as proposed in the Office Action, Applicant submits that such combination is not proper.

For the reasons stated above, Applicant submits that claim 1 is patentable over Madhaven in view of Ho and Ho ('251). Claims 9, 15, 22, 26, 30, and 33 recite similar elements as claim 1, and are patentable over Madhaven in view of Ho and Ho ('251) for the reasons stated above and additionally in view of the further elements recited in these independent claims.

Claims 2-8, 10-14, 16-21, 23-25, 27-29, 31-32, and 34-36 depend, directly or indirectly, on claims 1, 9, 15, 22, 26, 30, and 33, respectively, and are patentable over Madhaven in view of Ho and Ho ('251) for the reasons stated above and additionally in view of the further elements recited in these dependent claims.

Applicant respectfully requests withdrawal of these rejections of claims 1-36, and reconsideration and allowance of these claims.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 29 April '04

By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 29 day of April, 2004.

Tina Kolwit

Name

Signature